

Simulation Approach Aids RF Design Debugging

A single software tool performs all the analysis and synthesis functions needed to check RF design architectures and save valuable design cycles.

Design time can be dramatically shaved with the help of a new simulation technique that enables RF designers to perform root-cause analysis of RF architectures. The approach provides complete spectrum identification and origination information for each design, and allows arbitrary topologies and multiple signal paths to be explored. Based on a single software tool, continuous verification from the RF archite-

ture phase through the measured data phase can now be performed. When developing an RF architecture, an engineer determines the type, number, and order of stages needed to meet a set of requirements. Spread-

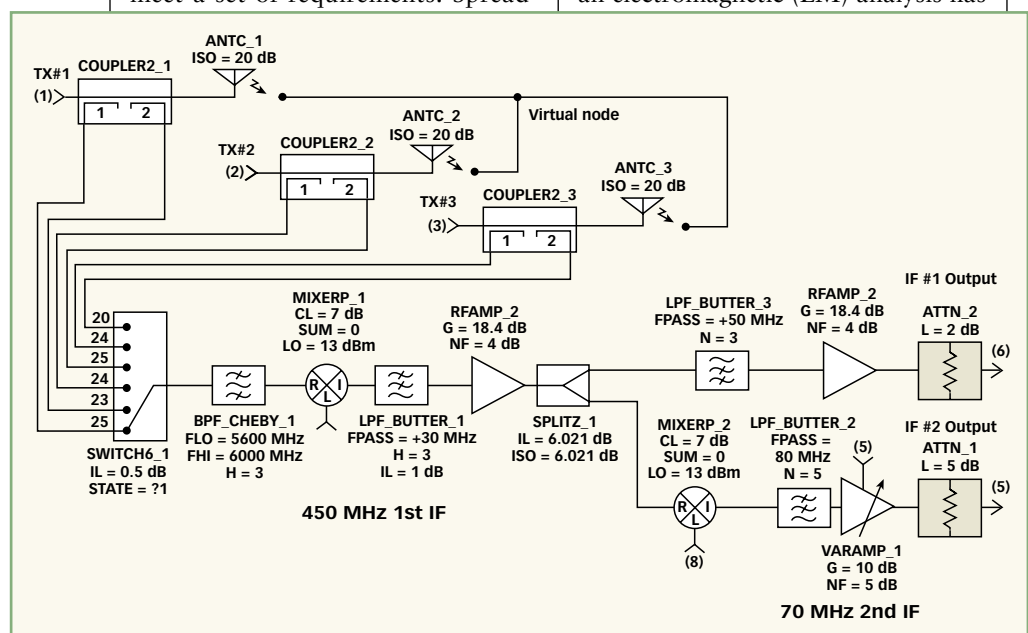
sheet software such as Microsoft Excel have typically been used for this design task, but the approach is inexact and can

lead to a poor RF architecture which will then present problems and lead to long product-development cycles. Design cycles typically occur when the basic RF architecture must be modified, or because an electromagnetic (EM) analysis has

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1. This block diagram shows a three-sector 5.8-GHz power/VSWR tester.

- Analyze “sneak” or leakage paths;
- Account for nonlinear behavior;
- Simulate broadband noise;
- Provide architectural optimization; and
- Simulate conducted emissions.

These features are part of a new sim-

ulation technique implemented in the SPECTRASYS module of the GENESYS suite of RF design software tools from Eagleware Corp. (Norcross, GA).

An example may help to illustrate how effective RF architecture analysis can save design time, using a three-sector 5.8-GHz

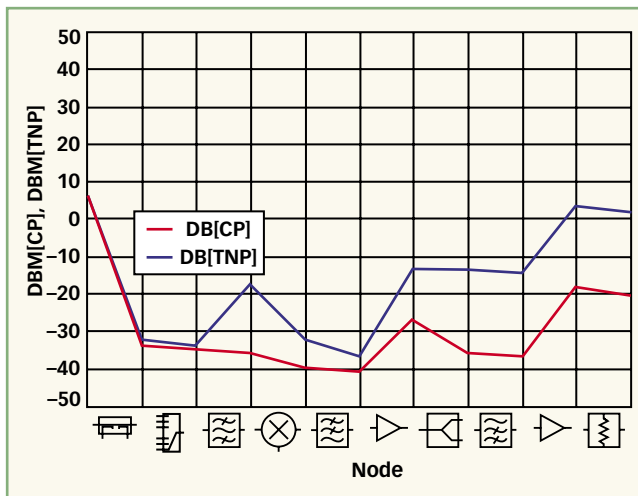
wireless-local-area-network (WLAN) VSWR/power tester (**Fig. 1**). In this design, a switchable receiver measures forward and reflected power for each of three antennas. The impedance of each antenna has been defined in terms of return loss. The first intermediate frequency (IF) is 450 MHz with no automatic-gain-control (AGC) stage. Consequently, this output can be used for actual power measurements. The second IF is at 70 MHz and has AGC. The second IF can be used as a demodulated output.

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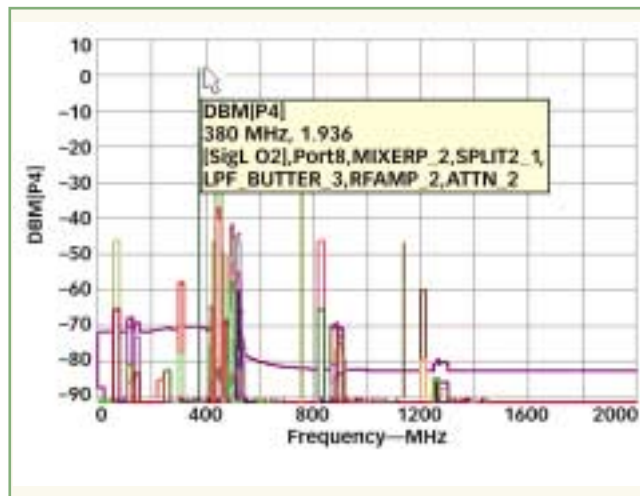
Figure 2 shows a WLAN modulation source applied to each antenna through a coupler. A virtual node has been created between antennas to represent antenna-to-antenna isolation. In this example, the dynamic range of the WLAN input signal is assumed to be between +10 and +30 dBm. This tester must accurately measure VSWR across this dynamic range for both the forward and reflected power.

The high-power case occurs when looking at the forward power of +30 dBm. **Figure 3** is a level diagram showing the total node power compared with the 1-dB compression point for each node, indicating that the last amplifier is in compression (the schematic symbol also changes color indicating an error). The graph makes helps to identify all of the weak links in this headroom chain.

The low-power case occurs when looking at the reflected power at the input power of +10 dBm. **Figure 4** shows a level diagram showing the total power at the node compared to the power in



4. By simulating the total power at the first IF node compared to the power in a 22-MHz WLAN channel, potential problems can be found with the design of Fig. 1.



5. By examining the spectrum of the first IF output port, offending signals can be identified.

a 22-MHz WLAN channel. By examining the total power at that point (the anticipated channel power), rather than with a power meter placed at the output port, a problem signal becomes apparent.

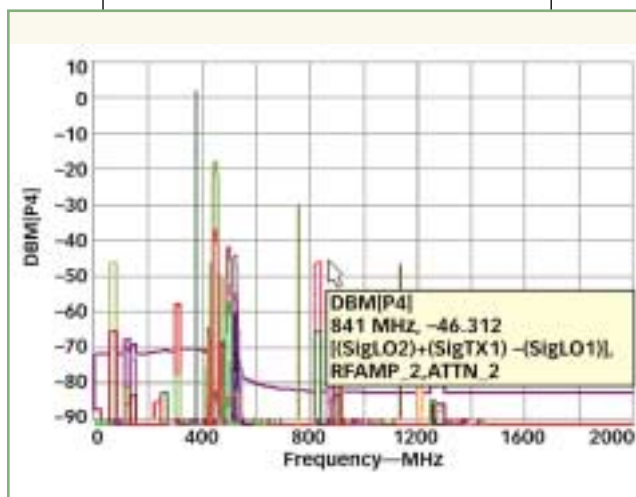
Once a problem is known, the next step is finding the root cause of the problem. By checking the first IF output spectrum in Fig. 5, the offending signal can be identified at a frequency of 380 MHz, power level of +1.936 dBm, equation of [SigLO2] (which is the name of the second LO source), a creating element of “Port8,” and a traveled path to the viewing node. The root cause of the problem is the second LO signal leaking into the output of the first IF section.

Figure 6 shows another identification example, in which a second-order intermodulation product is generated in “RFAMP_2” between the second LO (“SigLO2”) and the difference IF output (“SigTX1 – SigLO1”). By identifying additional spectrum, another root problem with this RF architecture becomes apparent: intermodulation generate in the first IF amplifier (“RFAMP_2”) by the 450-MHz IF signal and the second LO signal.

The best solution to this problem can be found by taking a close look at the path of the offending signal (Fig. 7). Corrective actions include reducing the LO drive to the second mixer, improving the LO-to-RF isolation of the second mixer, inserting a filter between the second mixer and splitter, improving the port-to-port isolation of the splitter, or using a bandpass filter instead of a lowpass filter in the first IF. Traditional analysis would not isolate this problem; it could only be found during laboratory tests of prototype hardware, thus requiring another design cycle.

Using the SPECTRASYS module of GENESYS, a designer can directly

invoke synthesis tools and design the sub-circuits directly from the behavioral model. The “corrective” bandpass filter, for example, can be synthesized using GENESYS’s FILTER module, with the synthesized circuit automatically substituted back into the RF architecture. The system simulation will then use this new circuit implementation for that stage of the RF architecture, rather than the behavioral model. Test or EM data for each component can easily be used in place of the behavior model by simply bringing up the component parameters and selecting the EM simulation or appropriate data file. This process of moving between behavioral, circuit, EM, and measured data enables continuous design verification, beginning with RF architecture all the way through measured data.



6. By performing identification of intermodulation signals, the root cause of the distortion can be found.

Accurate Models

Accurate models are important in any type of simulator. One of the major factors in producing a good RF architecture tool is the ability to simulate conducted emissions (for regulatory requirements such as those established by the FCC and ETSI). Traditional simulators make unilateral

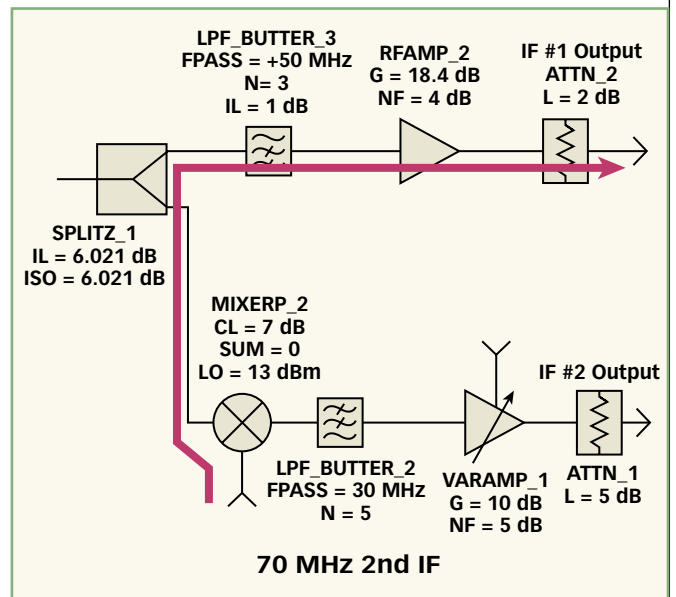
assumptions for system models and signals only flow in a single direction. The new simulation technique is based on bilateral models, which provide a more accurate prediction of conducted emissions. For example, a traditional simulator will assume that $S_{12} = 0$ for a system-level RF amplifier model to represent a case of perfect isolation, but such a condition cannot be used to accurately simulate conducted

emissions since an LO signal would never leak backward through the LNA and appear at the antenna. The bilateral approach allows for this leakage and consequently allows for a more accurate simulation of the leakage paths.

Since a number of components within a wireless design exhibit nonlinear behavior under certain conditions, traditional linear simulation falls short for RF architectural analysis. Harmonic-balance techniques are effective for nonlinear circuit simulation, but are limited because of their use of discrete (rather than continuous or swept) frequencies, lack of signal bandwidth, and lack of continuous noise or channel concept. Furthermore, convergence and the slow simulation speeds of harmonic-balance simulators can limit their usefulness. Simulating more than a handful of carriers can quickly become time consuming.

Time Simulations

Discrete time simulations are well suited for digital-signal-processing (DSP) design, although such simulations are based on narrowband assumptions when applied to RF design. This assumption ignores all of the spurious effects



7. This closeup view of the 70-MHz second IF section shows the root source of the offending signals (second LO signals leaking back into the first IF).

the designer is trying to identify and characterize. For example, an unwieldy number of simulation points are necessary to examine a 30-kHz signal on a 5-GHz carrier, not to mention the number of simulation points needed to examine the carrier's harmonics. In a discrete time simulation, the simulation time increases as the resolution is improved and/or the simulation frequency is increased. Furthermore, discrete time models typically contain no input and output impedance information, so VSWR cannot be included as part of a simulation. Having dedicated input and output ports also becomes a problem, because signals cannot travel backward through these models.

The new simulation approach provides the opportunity to model nonlinear behavior, but in a timely fashion. The approach provides RF architecture debugging and continuous design verification. It delivers complete spectrum identification and origination information for every spectrum, and accounts for VSW, leakage paths, broadband noise, and nonlinearities. For more information on the approach, including design examples in video form, visit the Eagleware website at www.eagleware.com. **MRF**