

# Alias (Spur) Reduction in Sampled Systems using the 32-bit version of SystemView by ELANIX

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## Introduction

This application note is specific the PLL-DIF.SVU example file and its related application note AN102A -- PLL Hardware Design and Software Simulation. However, it also applies to other areas of simulation and Digital Signal Processing (DSP) design such as the Analog-to-Digital Converter (ADC).

In the PLL example the output of the VCO metasytem is a square wave. The power spectrum of this signal (**Figure 2**) has a strong spectral line at 12.8 MHz, the locked-in frequency. Several lower amplitude spurs are also visible. These spurs are not present when an analog spectrum analyzer is used on a breadboard. In SystemView by ELANIX they are the result of the interaction of the square wave harmonics with the system sample rate (56 MHz). The sampling process produces alias frequencies that fall in the plotted Nyquist bandwidth. DSP designs and any system with a sampling ADC input have to reduce these aliases to an acceptable level.

PLL's are not normally considered to be a sampled system (except for the phase/frequency detector component). The designer does not expect to see any aliases in the plot of the spectral output. Since any system modeled in SystemView becomes a sampled system, what can be done to reduce the aliasing?

Three ways to reduce aliasing in sampled systems will be demonstrated.

1. Increasing the system sample rate.
2. Adding a noise source to the VCO's input causing its harmonics to dither or spread.
3. Eliminate the high frequency content of the signal by adding an anti-aliasing filter, thereby reducing the signal bandwidth.

## Increasing the Sample Rate

Increasing the sample rate and the number of samples (to maintain the same frequency resolution) helps to give a more detailed display. Sine waves become smoother, and edge transitions are steeper. The tradeoff is a longer simulation time, and possibly running out of computer memory resources. All of the simulations shown here were done on a 100 MHz / 16 MHz RAM Pentium. **Figures 1 through 5** show the effects of using increasingly faster sampling rates. Each time the rate was doubled, the number of samples was doubled to keep the *Time* window about 73 uSec wide. With each sample rate increase fewer aliasing spurs are noticeable. With 65,536 samples at 896 Mps (**Figure 5**) the last sharp spur was eliminated. A simulation run was also done with 131,072 samples at 1,792 Mps with good results.

## Adding a Noise Source

Another, more efficient, way of reducing the effects of aliasing in the simulation is to add a small amount of Gaussian noise to the input of the VCO (**Figure 9**). The noise causes the VCO's harmonics to dither or spread their power, especially at the higher frequencies. **Figures 6, 7, and 8** show the effects of using increasingly faster sampling rates. The noise was set to 0.1 volt<sub>rms</sub> in each case. Notice that 16,384 samples with noise gives about the same results as 65,536 samples without noise (**Figures 5 vs 8**). This technique of adding noise also works in the hardware world of A/D Converters. NOISE/COM, Inc. has an application note (**Ref. 1**) on selecting a noise diode for this purpose.

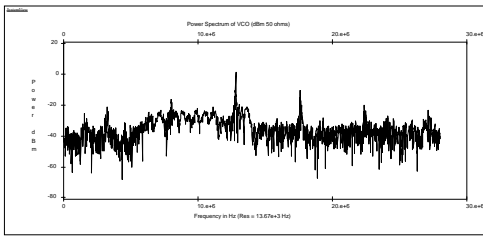


Figure 1. 4,096 samples, 56 MspS  
Undesired spurs: 1.5 3.2 8.0 17.6 22.4 27.1

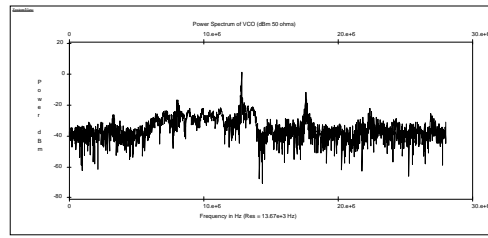


Figure 6. 4,096 samples, 56 MspS (0.10 V<sub>rms</sub> noise)  
Undesired spurs: 3.2 8.0 17.6 22.4

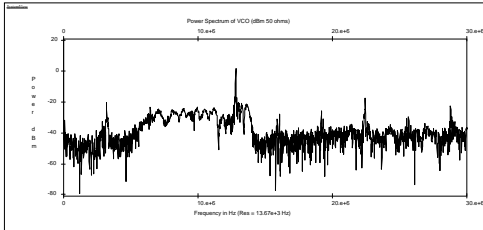


Figure 2. 8,192 samples, 112 MspS  
Undesired spurs: 3.2 19.2 22.4 25.7 28.8

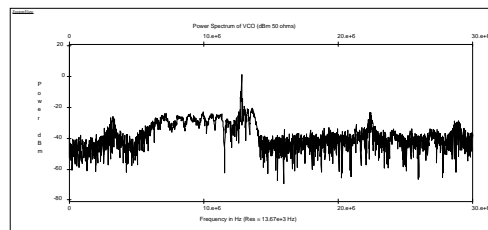


Figure 7. 8,192 samples, 112 MspS (0.10 V<sub>rms</sub> noise)  
Undesired spurs: 3.2 22.4 28.8

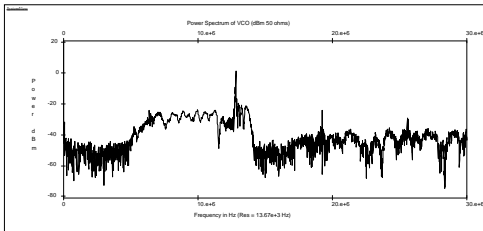


Figure 3. 16,384 samples, 224 MspS  
Undesired spurs: 19.2 25.6

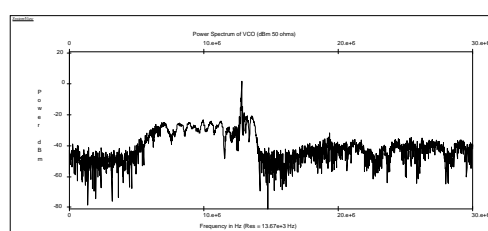


Figure 8. 16,384 samples, 224 MspS (0.10 V<sub>rms</sub> noise)  
No undesired spurs.

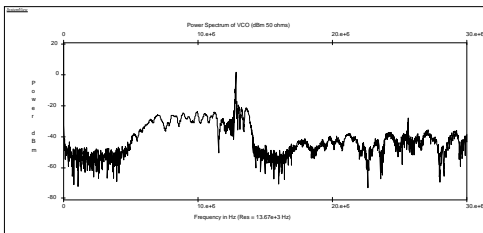


Figure 4. 32,768 samples, 448 MspS  
Undesired spur: 25.6

Figures 10, 11, and 12 Show a test system for the VCO metasystem, with and without noise added to its input. The results of this test indicate that noise added to the input can reduce the spectral power of the harmonics due to aliasing. The tradeoff for this improvement is a higher noise floor.

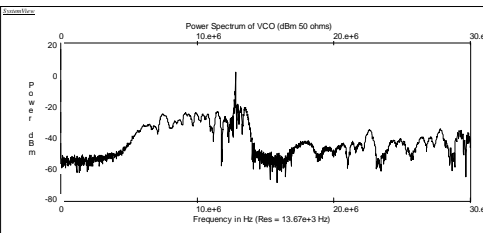


Figure 5. 65,536 samples, 986 MspS  
No undesired spurs.

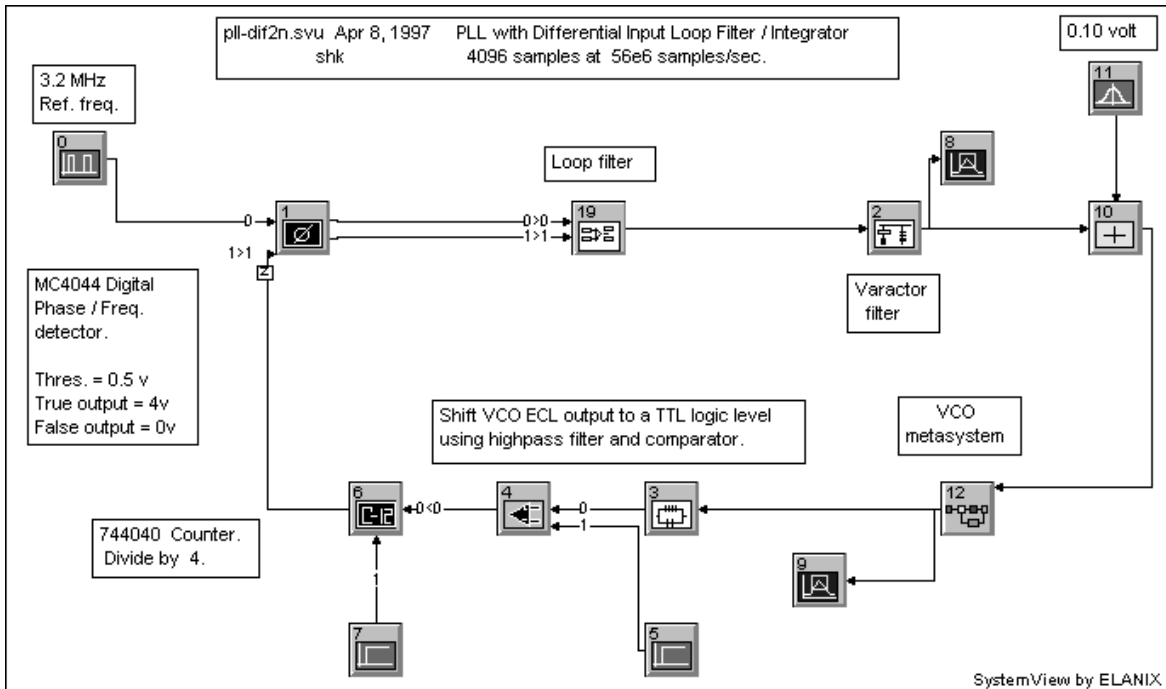


Figure 9. The PLL system with 0.10 volt<sub>rms</sub> noise added to the VCO.

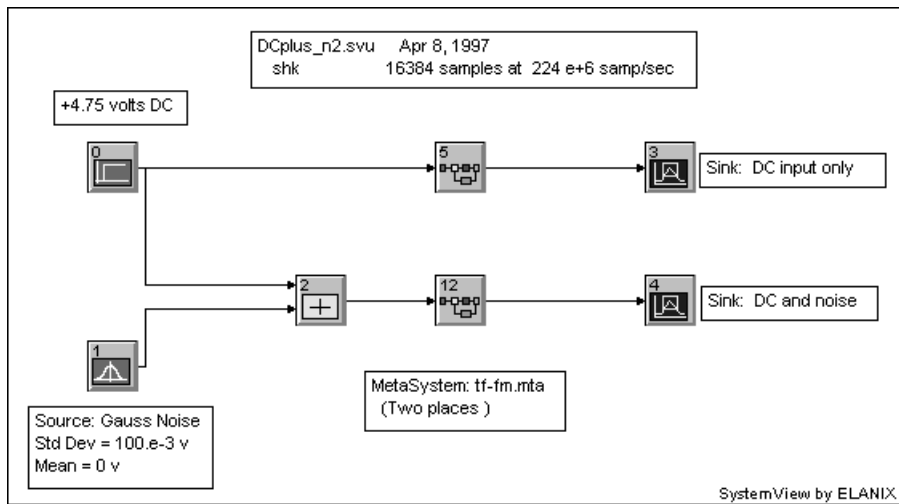


Figure 10. The VCO metasystem test system, with and without input noise

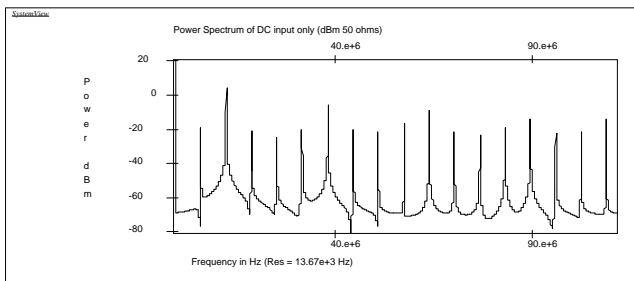


Figure 11. DC input only to the VCO.

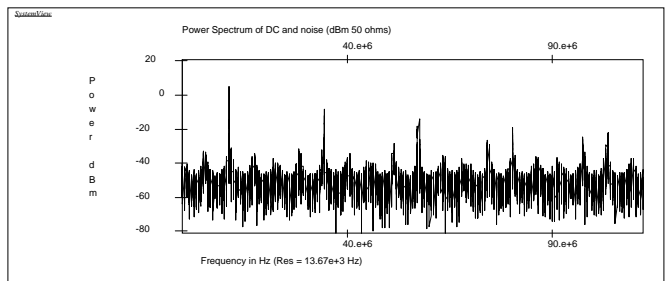


Figure 12. Both DC and 0.10 volt<sub>rms</sub> noise input to the VCO.

### Reducing the Signal Bandwidth

The 3rd, and probably the most important, way of reducing aliasing in a sampled system is to reduce the bandwidth of the incoming signal. **Figure 13** shows a typical front end of a DSP system. The filter is designed to reduce any offending high frequency input to the system. Manufacturers of signal processing components generally have detailed information on designing these systems. (Ref. 2)

Now, back to the PLL simulation example. The origin of the spurs is in the square wave output of the limiter token inside the VCO metasystem. It is possible to simplify the original PLL example and still get the same lock-in time response while eliminating the spurs. **Figure 14** shows the simplified PLL. First the limiter and polynomial tokens were deleted from the VCO metasystem. Then, in the main

system, the highpass filter and analog comparator were removed. Finally, the metasystem was “exploded” and cleaned up as shown. The output of the FM token is a sinewave, centered at zero volts. Consequently, the threshold of the 744040 counter is set to zero volts. This in turn requires that the counter’s MR (Master Reset) input be some negative value (-1.0 volts). The results of running the simplified system are shown in **Figures 15** and **16**.

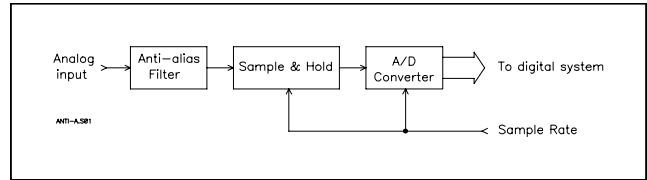


Figure 13. Typical hardware front end of a sampled data system.

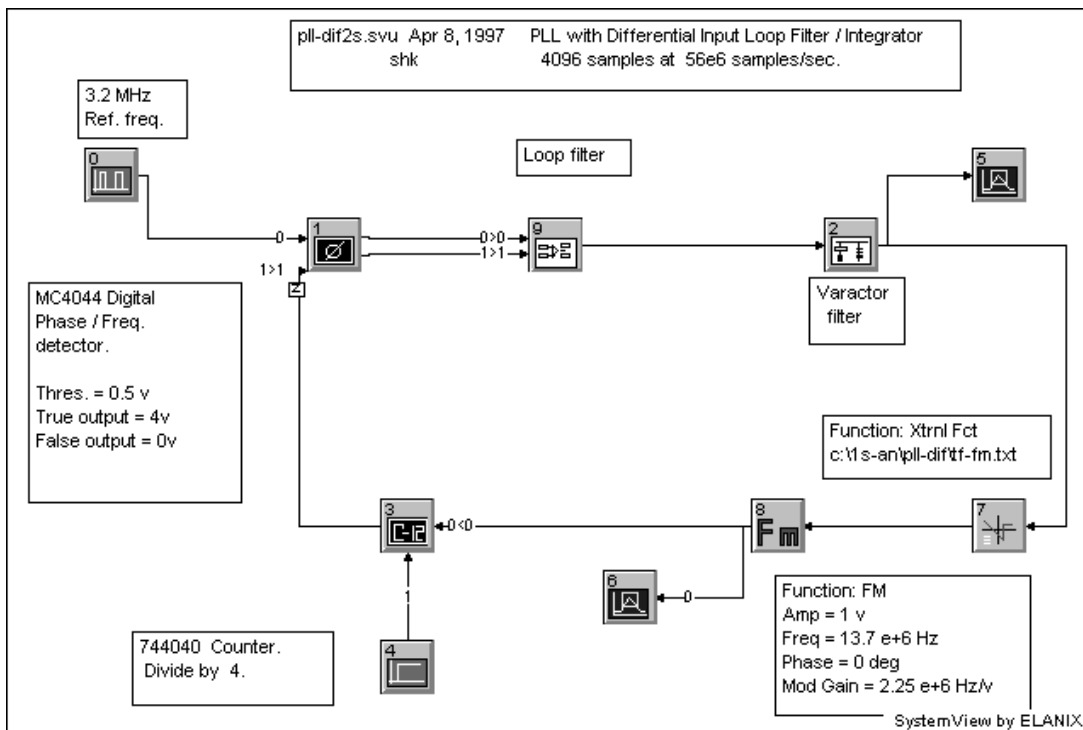


Figure 14. The original PLL without the -- limiter, poly, highpass filter, and analog comparator.

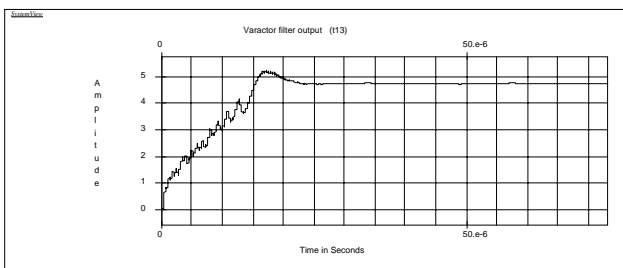


Figure 15. 4096 samples, 56 Msp PLL lock-up time with simplified system in Figure 14.

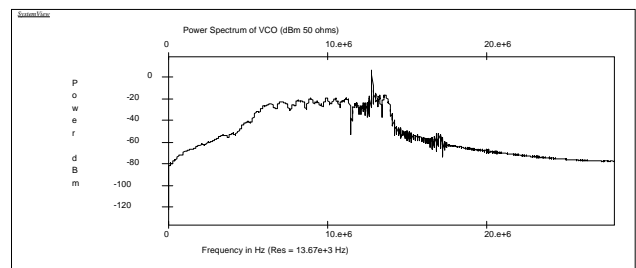


Figure 16. 4096 samples, 56 Msp VCO output with simplified system, no undesired spurs.

When **Figure 16** is compared with **Figure 5** we find that simplifying the VCO to have a sinewave output has dramatically reduced the simulation time (an FFT on 65,536 samples vs 4,096 samples). The VCO's sine wave output gives a "clean" FFT result. However, if a FFT is required on a counter (divider) output, we are again faced with fast rise time edges that produce aliasing spurs. One may be tempted to filter the output of the counter, but this has the following difficulty. Besides reducing the amplitude of the spurs caused by aliasing, the amplitude of the true spurs (3rd, 5th, 7th, etc., harmonics) will also be diminished. Also, the alias spurs that are in the passband of the filter will not be reduced in amplitude.

### **Conclusion**

Three ways to reduce aliasing in sampled systems have been shown.

1. Increasing the system sample rate.
2. Adding a noise source to the system to dither or spread the power of the harmonics.
3. And for a particular PLL system, the signal bandwidth was reduced by replacing the VCO square wave output with a sine wave output.

### **More Information**

For more information on SystemView simulation software please contact:

ELANIX, Inc.  
5655 Lindero Canyon Road, Suite 721  
Westlake Village CA 91362.  
Tel: (818) 597-1414  
Fax: (818) 597-1427

Or visit our web home page ( <http://www.elanix.com> ) to download an evaluation version of the software that can these simulations as well as other user entered designs.

### **References**

1. NOISE/COM, Inc., Noise Application Note 109, "Noise Diodes Randomize Quantization Errors in A/D Converters"
2. Analog Devices, Inc. "Mixed-Signal Design Seminar", Section III, Seminar Book: G1516-10-2/91